DisplayPort Interface

for Chrome 400/500 Series Graphics Processors

A S3 Graphics White Paper

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Revision History

B.0	11/11/2008	Added Chrome 500 Series GPU Support	BT/KG
A.0	7/26/2007	Initial Version	BT/KG

Introduction

This White Paper provides an overview of the Video Electronic Standards Association (VESA).DisplayPort Interface Standard. DisplayPort is a scalable digital display interface targeting internal (notebook LCD panels) and external (device-to-device) display connections. DisplayPort capabilities make it possible to enable higher levels of display quality and additional display features to enhance the user's high-definition (HD) cinematic experience. The standard is open and royalty-free to all VESA member and non-member technology vendors, and any specification improvements and changes are governed by the DisplayPort standards body and thus are transparent for users to adopt.

The technology introduced by DisplayPort enables the transition to the next generation display interface and moves away from the combination of analog/digital signals to a purely digital interface. Digital signals have innate characteristics from a technological, visual, and cost standpoint that provide numerous advantages. S3 Graphics Chrome 400/500 Series processors support the DisplayPort interface to give viewers the ultimate visual experience.

DisplayPort Overview

DisplayPort signaling uses a serial “micro-packet” architecture, similar to PCI Express, to provide high bandwidth and greater color depths to drive high resolution monitors with increased realism and color range. The standard supports and unifies all features found in previous display technologies, but takes the technology one step further by allowing audio to be embedded in the DisplayPort data stream so that one cable carries both audio and video (A/V) data streams. In addition, DisplayPort incorporates a layer of copyright protection for content to be viewed and transmitted securely, providing protection for intellectual property owners from piracy and misuse of protected material. Figure 1 illustrates a notebook sample implementation for DisplayPort, where the graphics processor natively and directly drives the LCD panel through one DisplayPort (embedded DisplayPort or eDP) connection, while a second DisplayPort connection is available from the notebook to an external monitor or digital TV. Other notebook display connectors such as connectors for VGA, TV-out (S-Video), and DVI, can be replaced by DisplayPort, saving valuable space as well as saving the cost of providing a range of connectors specific to different display technology standards.

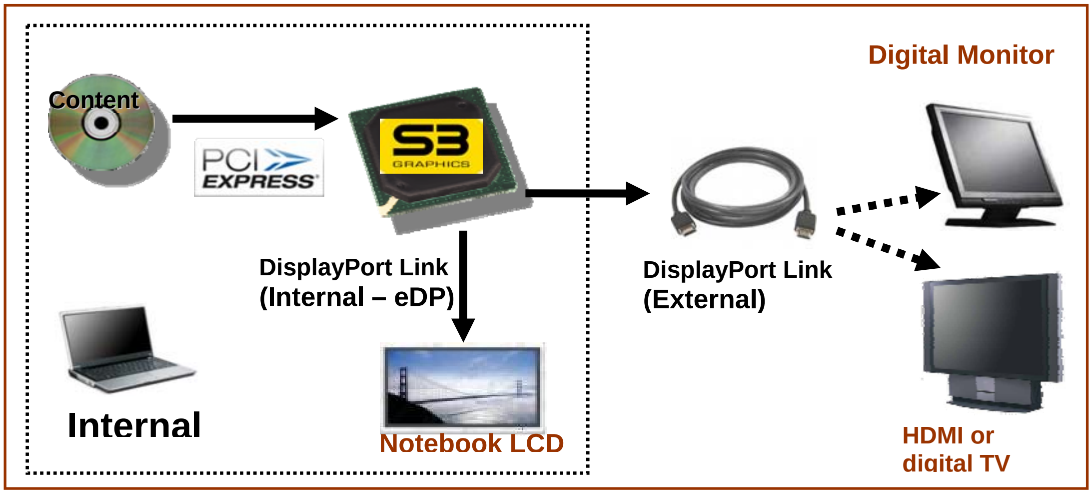

Figure 1: DisplayPort Notebook Connectivity Example

Drawbacks of Other Display Technologies

VGA Limitations

For a long time VGA (RGB) was the standard analog display interface that most desktops computers traditionally used to connect to a monitor. The problem with this technology is that it used large and bulky CRT monitors that increase in size and weight as the resolution increases. Thinner digital flat panel monitors now in the market are capable of inputting RGB signals, but additional circuitry and analog-to-digital conversion (ADC) chips are needed to convert RGB data to digital data. This increases the cost to the monitor manufacturer and end user. In addition, the ADC process is lossy, causing screen detail loss. The refresh rate of the monitor and non-linear characteristics (gamma) affect viewing quality. CRT monitors are power hungry since the internal components consume a lot of power driving the display process. Finally, cable lengths are limited because of signal attenuation. Figure 2 shows a basic RGB connection between a graphics processor and monitor where the display data in the processor is converted from digital to analog (via the RAMDAC) and then back to digital.

DVI Limitations

DVI is a digital format using transition-minimized differential signals (TMDS) that overcome most of the RGB drawbacks. DVI connectors can be found on desktop, notebook, and consumer electronic (CE) devices such as digital TV sets. Since the graphics processor processes display data in the digital domain, DVI keeps the display data in digital format throughout the display pipeline from processor through to the display monitor.

Even though DVI is a digital format, there are numerous drawbacks.

- **DVI specification is frozen:**
  - The Digital Display Working Group (DDWG) which oversaw the DVI specification, has split up, so there is no longer a governing body to oversee any specification upgrades, extensions, or improvements to the latest 1.0 version.
  - Color depth, bandwidth, and resolution are all set by the standard, preventing standardized support for higher resolution monitors introduced into the market. If higher resolutions are needed, the GPU can incorporate two DVI transmitters to provide a dual-link DVI connection at additional chip cost (die size, mixed signal blocks, testing) and royalties.

- **DVI conversion to LVDS:** Even though the DVI display pipeline is digital, flat panels use LVDS technology for the display, so DVI needs to be converted to LVDS before being used. Flat panel monitors include a DVI receiver chip to provide this conversion, which adds additional circuitry and component costs.

- **Royalty / licensing fees:** Adopters are required to pay royalties for DVI and licensing fees for optional content protection (HDCP) support.

- **Large connector size:** DVI connectors are not optimal for notebook or small form factor designs, because of the large space requirements for the connector.

- **PCB level issues:**
    - o DVI can be a source of electromagnetic interference (EMI) at higher pixel clock frequencies when driving higher resolution displays.
    - o Since the display data differential pairs are separate from the clock differential pair, trace length routing and inter/intra-pair signal routing are critical to avoid trace length mismatches and signal timing skew.
    - o The DC-coupled signal voltage levels are not compatible when using DVI transmitters and receivers at different process technologies since they use different voltage levels.

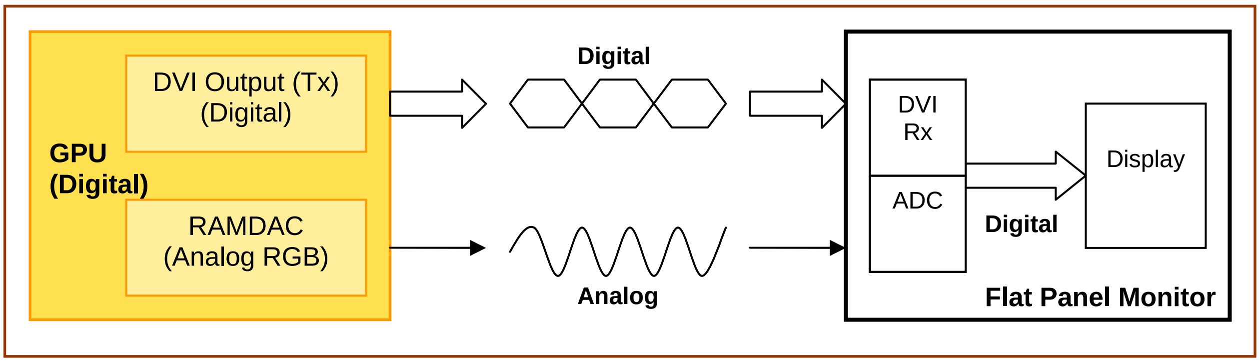

Figure 2: RGB and DVI Connection (Simplified)

LVDS Limitations

Low-voltage differential signaling (LVDS) is the de-facto digital standard used in notebook computers to connect the GPU to the LCD panel. The disadvantages of LVDS are:

- **Scalability:** LVDS requires additional data pairs as resolution size increases. In notebook designs, hinges contain the LVDS wires in addition to other wiring for devices such as wireless Wi-Fi antennas or built-in camera modules. As notebook functionality increases, the hinges become more of a gating factor for the expansion of LCD panel resolution.

- **Clock limited:** LVDS has strict timing requirements between the data pairs and clock signal, so any timing skew or clock/data jitter will reduce the data sampling window and introduce timing and display errors. This limitation reduces the distance LVDS can travel to short distances only.

HDMI Limitations

High-definition multimedia interface (HDMI) is based on the TMDS signaling protocol and is a superset of DVI technology. HDMI is popular in the consumer electronics market and is used in devices such as TV sets, DVD players, and set-top boxes because it provides benefits beyond other existing consumer display technologies. HDMI technology is scalable in terms of bandwidth and resolution. Updates to the specification are still being made, with the latest HDMI release providing support for even more features and higher performance, while maintaining backwards compatibility with older versions of HDMI and DVI. Like DisplayPort, HDMI supports audio streams that can be encoded into the data stream so one cable can support audio and video streams across a secure connection using HDCP. Since HDMI has the same topology as DVI (with separate clock and data signals), design limitations found in DVI, such as clock/timing skew, EMI, and routing issues, still exist in HDMI.

Because of high implementation costs associated with this technology's royalties and IP, HDMI initially had only a small user base in the PC market. With few early PC adopters strongly supporting this display connection, along with eroding average selling prices (ASP) for their units, it was hard for HDMI to make early inroads in the PC space. Over time the cost of using this technology has decreased as CE implementers increased and more display devices incorporated this interface. The current transition of the PC to an entertainment media device connecting directly to television sets has allowed HDMI to make progress in the PC space as more graphics processors support this interface. With both HDMI and DisplayPort capability, the S3 Graphics Chrome 400/500 Series graphics processors are flexible enough to support both PC and CE displays.

Note: Please refer to the S3 Graphics HDMI white paper for more information on this technology.

Benefits of DisplayPort

DisplayPort overcomes the inherent drawbacks of VGA/DVI/LVDS with the following:

- **High-definition (HD) viewing:** A goal of DisplayPort is to give viewers the ultimate HD multimedia (audio and video) experience as media content advances to HD quality (e.g, movies on Blu-Ray™ Disc). Chrome 400/500 Series processors are capable of inputting HD or I2S audio signals and encoding the audio stream along with the display stream to fully support the DisplayPort A/V standard.

- **Unified display architecture:** Internal (inside-the-box, eDP) and external (box-to-box) devices can use the same technology to meet all user needs, avoiding mixing-and-matching of different standards and technologies for displays.

- **Scalable performance:** Increases in performance, color depth support, resolution, and feature support allow changes to be made at the Physical Layer (described below), permitting backwards compatibility using the same connectors and older/newer devices. The architecture is modularized so changes can be made to one block without affecting functionality of other blocks.

- **Comprehensive interface:** The signaling technology lets the data pairs transmit video (display) data, audio data, and auxiliary data to allow full communication with each display device. DisplayPort's goal is to replace multiple A/V cables with one simple user-friendly cable to connect different types of devices. A single cable can operate up to 15-meters (longer if using DisplayPort repeaters) so the user is not confined by distance as with other technologies. For example, an overhead projector in a large conference room can have its DisplayPort cable routed from input in a side wall to the center of the room where a laptop with presentation material sits.

- **Simple board-level design:** The data signals have the clock embedded in 8B/10B encoding where the DisplayPort transmitter converts 8-bits to 10-bits for transmission, and the receiver converts the 10-bits back to 8-bits for display. The extra 2-bit overhead allows enough state changes so that the receiver can extract the embedded clock signal correctly and recover the data. This implementation allows the PCB/cable routing to be more relaxed since the data and clock signals are not routed separately, and helps prevent data-clock synchronization problems and skew on the PCB level. There are also fewer signals (wires) for a lower pin-count allowing simpler platform design. For example, WSXGA+ (1680 x 1050 resolution) support at 18-bits/pixel would require eight LVDS pairs, four DVI (TMDS) pairs instead of just one DisplayPort (eDP) pair.

- **Small form factor:** The connector in Figure 3 is significantly smaller than a DVI or VGA connector. The small form factor saves valuable space in notebooks and desktops and allows for more connectors per area for multiple display connections.

- **Increasing user base:** The adoption of DisplayPort by major PC and CE OEMs/manufacturers has provided viability and support for this technology.

- **Low cost:** DisplayPort is an open-standard available to all users and adopters without any royalties. The nature of the technology also removes costly logic and conversion chips needed in flat panels (ADC, DVI Receiver) so overall cost is reduced. In addition, the standard is trying to integrate all of the display functions into the chip level to reduce external device complexity.

- **VESA support:** VESA is the de facto display standards organization in the PC market. They have strict compliance testing and implementation programs for logos and certification, to ensure interoperability between devices as the user base expands rapidly.

- **Multi-Display flexibility:** VESA has taken the initiative to make DisplayPort a multi-display standard providing a flexible interface to support HDMI/DVI/VGA via an external DisplayPort-to-DVI/HDMI/VGA dongle, allowing display extensibility and legacy support. Through an external active protocol dongle, a DisplayPort signal can be converted to DVI (single/dual-link), HDMI (including audio), and/or VGA. This flexibility allows a user with DisplayPort to connect universally to other devices, regardless of the interface. The converter in the dongle can be directly powered using the DP_PWR pin defined on the connector.

  Note: Please refer to VESA's DisplayPort Interoperability Guideline for more information about multi-display interface standard support.

- **Content protection:** DisplayPort supports DPCP (DisplayPort Content Protection) and HDCP 1.3 (High-bandwidth Digital Content Protection) to ensure secured transmission across all levels of the display connections.

  - **DPCP:** Developed by Philips and based on 128-bit AES encryption. Each individual connection (e.g., watching movies on a TV with a PC) is authenticated with a unique session key that creates a secure point-to-point connection. This connection is constantly monitored to ensure the connection is not compromised or bypassed for unauthorized users to view or copy. If the connection is deemed insecure, the DPCP will revoke the session key and users will not be able to play content at the full HD quality level.

  - **HDCP:** HDCP works similar to DPCP, where the connection is authenticated to determine if the receiver is licensed to receive HD content from the source. Each device has 40 unique 56-bit secret keys (Device Private Keys) and an identifier (KSV) that is 40-bits long. During authentication the transmitter (Tx) will request the KSV of the receiver (Rx) and determine if it is valid. If the KSVs are valid then the Rx and Tx each create a 56-bit shared secret value using the other device's KSV. Based on the decoding of the shared secret value each device can determine if the connection is legal. If it is not, the user can still view the media content, but at low quality. If the connection is between two authenticated HDCP devices, then the full quality available with the HD output can be experienced. The Chrome 400/500 Series processors include an internal HDCP keystore and logic to decrypt the HDCP encryption on the fly. This key set can be shared between DisplayPort, DVI, and HDMI.

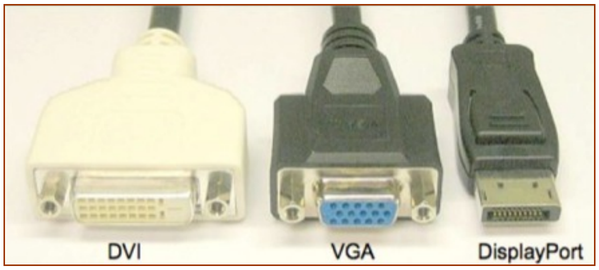

Figure 3: Display Connector Comparison (DVI / VGA / DisplayPort)

	DisplayPort 1.1	LVDS	DVI	HDMI 1.3
No. of Data/Clock Differential Pairs **1680x1050@18bpp** **1600x1200@30bpp** **2048x1536@36bpp**	1, 2, or 4 data No clock pair 1 pair 2 pairs 4 pairs	8 data (dual link) 2 clock (dual link) 4 pairs 12 pairs 14 pairs	3 or 6 data 1 clock 4 pairs 7 pairs N/A	3 or 6 data 1 clock 4 pairs 4 pairs 4 pairs
Bit rate per pair (Gbps)	1.6 or 2.7	0.945	1.65	1.65 to 3.4
Total Raw Capacity (Gbps)	1.6 to 10.8	7.56	4.95 (single link) to 9.9 (dual link)	4.95 to 10.2 (single link)
AC-Coupled for Process Migration	Yes	No	No	No
Audio Support	Yes	No	No	Yes
Auxiliary Channels	1Mbps AUX CH	No	DDC	DDC
Channel Coding	8B/10B	No	TMDS	TMDS
Content Protection	DPCP, HDCP 1.3 (Optional)	No	HDCP (Optional)	HDCP (Optional)
Signal Protocol	Micro-packet based	Sequential data stream	Serial data stream	Serial data stream
Internal (notebook) Connection	Yes	Notebook standard	No	No
Future Extensibility	Yes	No	No	Yes
Technology Royalty/Licensing	No	No	Yes	Yes
Content Protection Licensing	Yes	No	Yes	Yes
Multi-Display Interface Standard	Yes – with dongle (HDMI/DVI/VGA)	No	No	DVI
Controlling Authority	VESA	ANSI Standard	No (DDWG in the past)	HDMI LLC Promoter Group

Table 1: Comparison of Display Standards

DisplayPort Structure

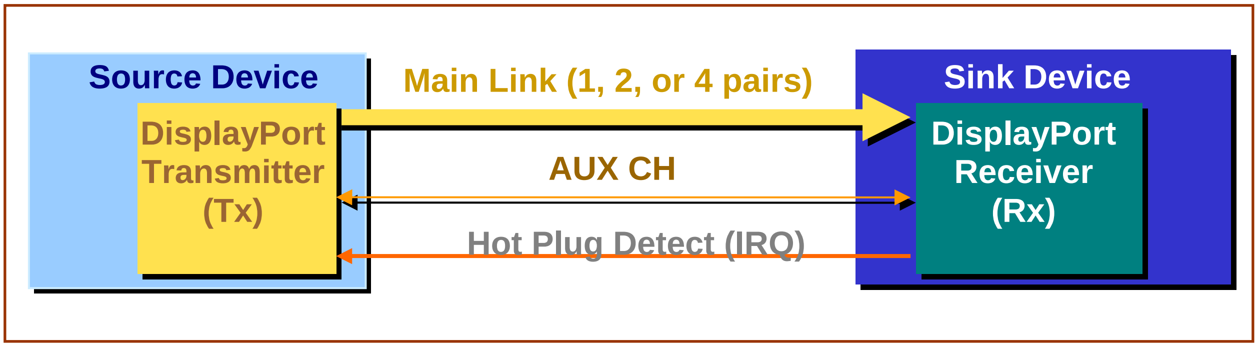

Figure 4: DisplayPort Structure and Signals

DisplayPort Signal Definitions

- **Main Link Signals:**
  - High-bandwidth, unidirectional, and low-latency signals
  - Isochronous transport of uncompressed audio and video streams
  - Clock embedded in data stream (8B/10B encoding)
    - No external clock or receiver reference clock needed
  - AC-coupled differential pairs
    - Different common mode voltages at Tx/Rx supported for different process technologies (ex. 0.35um vs. 0.18um vs. 0.065um devices)
  - Link can consist of 1, 2, or 4 lanes (data pairs)
  - Link rate per lane can be 1.62Gbps or 2.7Gbps
    - Link rate depends on channel quality and Tx/Rx support (silicon process)
    - Link rate is separate from pixel rate
    - Link rate = (# lanes) x (link rate per lane)
  - Supports 6, 8, 10, 12, and 16 bits per component (color)
  - EMI reduction
    - Data symbols (8B/10B encoded packets) are scrambled to reduce frequency hotspots (fixed serial bit patterns) and EMI emissions
  - Link training to support required number of lanes between Tx/Rx
  - Audio data
    - Audio packets can be transported during horizontal/vertical blanking
    - 6MB/s audio bandwidth

- **AUX CH (Auxiliary Channel):**
  - Low-latency and bi-directional signal
  - AC-coupled differential pair
  - Self-clocked data signal using Manchester II encoding
  - Performs link management and device control (DDC, EDID, MCCS)
  - 1Mbps data rate

- **Hot Plug Detect (HPD):**
  - A method of informing the system that an event (monitor connection, plugging/unplugging a monitor) has occurred.
  - The sink device will send an interrupt signal (HPD) to the source device that will in turn acknowledge the new device and configure the display output accordingly.

DisplayPort Architecture

The underlying architecture is modularized and layered allowing incremental improvements to take place in one block without affecting the others. For example, as signaling speeds increase in future versions of DisplayPort, changes can be made to the PHY (Physical) layer leaving the Link Layer and actual connectors untouched. The two blocks of the architecture are the Link and the PHY layers.

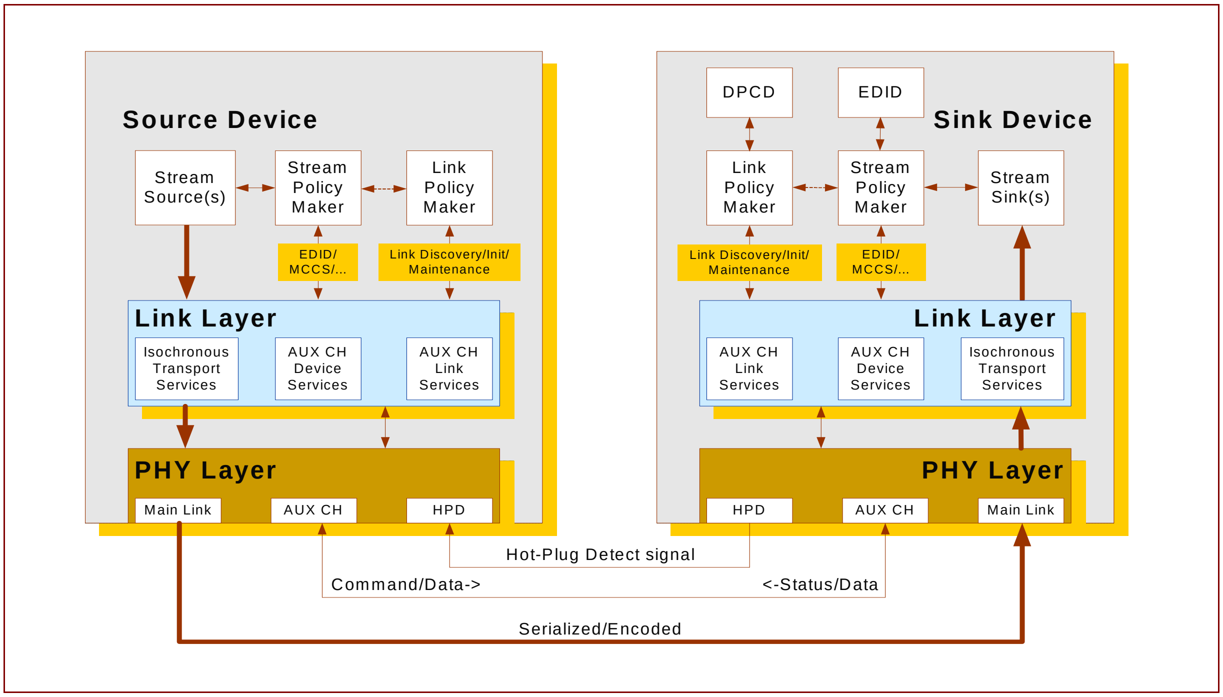

Figure 5: DisplayPort Layered Architecture

Link Layer

The Link Layer provides the following functions:

- **Isochronous Transport Services:** In the Source device, this feature maps the data stream to the corresponding Main Link lane so that the sink (receiver) can re-map and re-assemble the data to the original format, based on a specified algorithm. The data can be mapped based on the number of lanes, so that each lane gets equal loading for data transport efficiency. The actual data stream traveling across the Main Link is called a Transport Unit, which is made up of sixty-four link symbols per lane.

- **Link and Device Services:** Provides link management and device control. The source reads the receiver's DPCD (DisplayPort Configuration Data) through the AUX channel and configures and establishes the link connection (1, 2, or 4 lanes) through link training. There is also constant monitoring and communication between devices through MCCS/EDID/DDC commands to prevent display glitches such as the loss of synchronization.

Physical (PHY) Layer

The Physical Layer provides the following two functional blocks:

- **Logical sub-block:** This block scrambles and de-scrambles data sent across the Main Link for EMI reduction. It also performs encoding and decoding of the Main Link data stream (8B/10B) and AUX CH (Manchester II) based on the communications protocol.

- **Electrical sub-block:** This block contains the actual electrical circuitry for the differential pair links such as the SERDES (serializer/de-serializer) which takes parallel data streams in the GPU and converts them to a serial stream and vice versa. The transmitter/receiver and pre-emphasis/equalization for the Main Link are also found in this sub-block.

Possible Future DisplayPort Improvements

With a modularized architecture, the signaling layer of the DisplayPort devices can be improved without affecting any of the logical blocks in the Link Layer or the external connectors, while still maintaining backwards compatibility. Possible changes to the signaling layer could mean twice the bandwidth of today's connection at the Main Link and AUX CH. With increased bandwidth, higher resolution support such as 4096x2160 and color depths of 48bpp (billions of colors) at higher refresh rates could provide a flawless ultra HD viewing experience that goes beyond today's best picture quality, that of the DCI (Digital Cinema) standard set by the major motion movie producers. Additional HD channels or multiple screen (PiP) can effectively be viewed at full uncompressed data rates, and other functional features such as interactive communication (for example. Educational classrooms and interactive shopping) could also be supported. Upgrades to the AUX CH will allow a true sideband interface to carry additional data streams, for example, PC CAM/Webcam with audio.

Conclusion

The natural advancement towards digital displays with higher resolutions and stunning visuals has led to a new display standard which aims to overcome the limitations of today's technologies and bring users to the next step in graphics and video realism. Support for this technology from VESA as well as major PC and CE OEMs has enabled DisplayPort to become a reality, as DisplayPort is incorporated into shipping and upcoming product introductions.

S3 Graphics' commitment to provide the best-in-class viewing quality and features is reflected in the Chrome 400/500 Series graphics processors' support for the full functionality of DisplayPort, enabling seamless multimedia connectivity to DisplayPort compliant devices.